Monolithic Millimeterwave Frequency tripler using a 0.35 µm BiCMOS SiGe technology

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ABSTRACT — **In this paper, we present a 10/30 GHz MMIC tripler using a 0.35 µm, 60 GHz-f_{MAX} BiCMOS SiGe technology. It exhibits a conversion gain in the -5 dB range, a fundamental rejection between -12 and -24 dB over an input dynamic range of]-5; 3[dBm. A low additive phase noise of -143 dBc/Hz at a frequency offset of 100 kHz is anticipated. The DC power consumption is 440 mW. The chip surface is 800x650 µm² (0.4 mm² only without the probe pads area). In order to drive this tripler, the design of a MMIC SiGe X-band VCO and its measured performance (0.8 GHz tuning range, -5 dBm output power and – 87 dBc/Hz phase noise @ 100 kHz off carrier) is also reported.**

I. INTRODUCTION

It is understood that the microwave spectrum is getting to be very overcrowded and this turns out to an increase of the allocated frequency range for wireless applications in the millimetre wave range (>20 GHz). These last years, a new contender emerges for microwave applications: the SiGe technology. This technology features the advantages of silicon in terms of cost and maturity of the process and authorizes operating frequencies beyond 50 GHz. It further exhibits excellent properties in term of noise (both in the high frequency range for low noise amplifiers and in the low frequency range for low phase noise oscillators) due to the good quality of silicon materials, the low access resistance in the active base region, a low transit time as well as a high current gain. Moreover, the last developments of these technologies have made it possible to drastically improve the quality factors of inductors [1]. This allows the emergence in the MMIC market of very competitive circuits based on alloys of silicon-germanium [2].

A very critical point is related to the millimeter wave generation using low cost silicon-based technologies. This paper reports on an X-band oscillator followed by a frequency tripler. This configuration is indeed expected to provide good performance in term of phase noise.

A frequency tripler using a low complexity BiCMOS SiGe technology from ST Microelectronics is proposed. The available SiGe HBTs exhibit a graded Ge profile within the base in order to reduce the base transit time. The emitter width is 0.35 µm. The breakdown voltage can be adjusted through a selectively implanted collector between 5.5 V and 3.3 V. We will use the low voltage version exhibiting the higher f_{max} value (60 GHz). Such a device also exhibits a current gain of about 100 and an f_t value of 45 GHz. The nonlinear electrical behavior of the device is described through a modified "Gummel Poon" model. Concerning the passive elements, the technology features five metal levels, which makes possible the realization of MIM capacitances and spiral inductors featuring reasonable quality factor.

The next section addresses the tripler design work; the following one reports on tripler performance carried out from electrical simulations and measured data. The following one compares these data with previously published ones. The last but one section deals with the design and performance of an X-band MMIC VCO able to drive the tripler. Finally, conclusions will be outlined in the last section of this paper.

II. TRIPLER DESIGN

Frequency multiplication is an efficient method for low phase noise signal generation [3], [4], [5], and [6]. If the tripler residual phase noise is sufficiently low, the 10 GHz oscillator frequency fluctuations are simply multiplied by 3, which results in a phase noise degradation of 9,5 dB which is the minimum degradation that can be expected between a 10 GHz fundamental and a 30 GHz multiplied source. The topology of the frequency tripler circuit is depicted in Figure 1. The originality of the circuit is related to the cascode topology that has been implemented within the differential structure. Cascode topology was retained for various reasons: the cascode amplifier exhibits advantages in term of stability, isolation and frequency bandwidth.

The two cascode cells are assembled through a conventional differential topology in order to enhance high odd harmonics when the circuit is operated in the nonlinear

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regime. Third harmonic signal is filtered using an appropriate LC circuit.

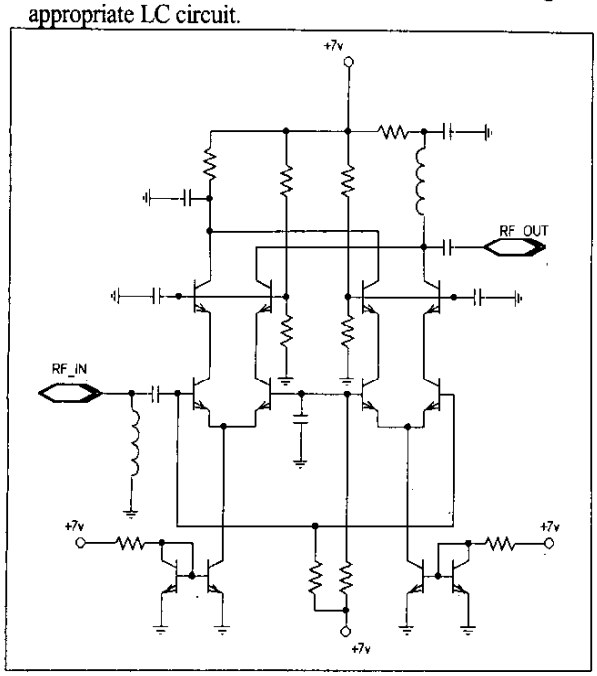

Fig. 1: Schematic topology of the frequency tripler

The layout of the circuit has been completed using Cadence software. The frequency tripler features a total DC bias voltage of 7 V and the total power consumption is 440 mW. The circuit has been processed by ST Microelectronics. Its layout is shown in Figure 2. The chip size is 800x650µm^2 and its useful area is in fact 600x650µm^2 (0.4 mm^2) if the microwave probe pads are not considered. Apart from minimizing the silicon surface, special attention has been paid in order to minimize the parasitics and top optimize the balancing behavior.

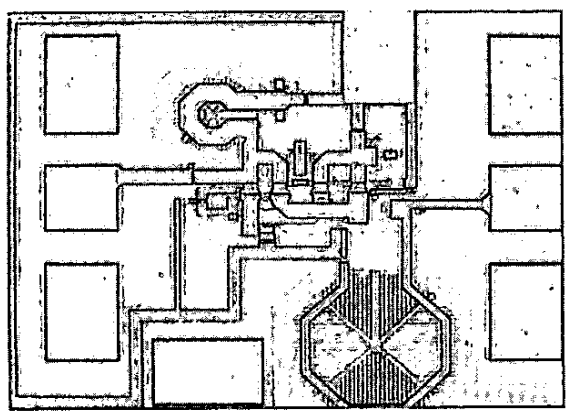

Fig. 2: Layout of the frequency tripler
(0.4 mm^2 if probe pads are not considered)

The next section will compare the simulated and measured electrical performance.

III. RESULTS

The design has been realized through the Agilent-ADS software and the STMicroelectronics's BiCMOS SiGe design kit. The computed and measured conversion gains together with fundamental and second order harmonics rejections versus input signal power (dBm) are depicted in Figure 3.

This simulation has firstly been carried out at a 10 GHz input signal. Results indicate a maximum conversion gain of about -5 dB and that an optimum circuit operation is achieved using an input power signal in the range of [-5; 4 dBm]. In this case, as displayed in figure 3, fundamental rejection ranges between –15 and –24 dB and second harmonic rejection ranges between –12 and –16 dBc are theoretically achieved.

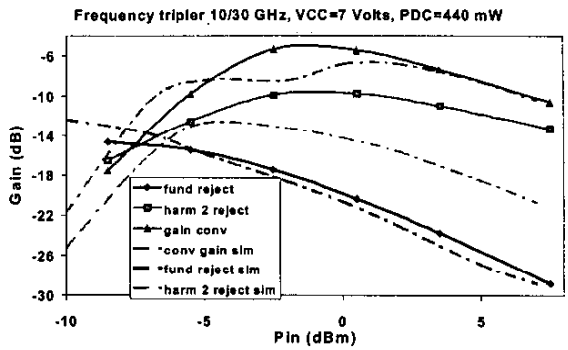

Fig. 3: Simulated and measured conversion gain, fundamental and harmonic 2 rejection versus input power (dBm) at 10 GHz input signal frequency.

Figure 3 shows that the computed conversion gain and fundamental rejection fit the measured data. The measured harmonic rejection is only 8 dBc. Such a value is excellent for an MMIC tripler which does not include a high Q output filter but is less than the predicted one. Observed differences originate from an inaccuracy in HBT's and passive elements models. Indeed these models were specified only up to 10 GHz at the time of the design. Therefore a new tripler design has now been completed using new updated 40 GHz models and its performance will be presented at the conference.

Further simulations have been completed in order to stimate the frequency tripler performance versus frequency ı the 9 to 11 GHz range. Figure 4 shows the variations of ıe simulated and measured conversion gain, fundamental nd second harmonic rejection for a 0 dBm input power. The omputed fundamental signal rejection is not less than – ₋0dB range and the second harmonic rejection ranges

between –18 and –14 dBc over the frequency bandwidth for an optimal input power.

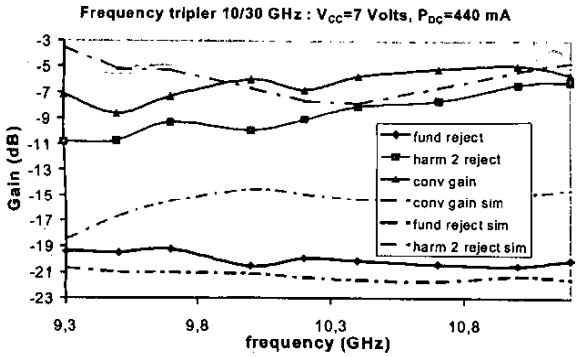

Fig. 4: Simulated and measured performance of the frequency tripler versus input frequency ranging from 9 to 11 GHz at a 0 dBm input power: conversion gain, fundamental and harmonic 2 rejection.

On wafer characterization versus frequency has also been performed. Conversion gain ranges from -7 to -5 dB as expected from simulations. We will give more detailed results concerning the spurious signal rejection in the extended version of the paper.

The last section of the paper will outline a comparison of our circuit with the state of the art and will address the phase noise behavior of such a frequency tripler which is a very important point for the design of a low phase noise millimeter wave source.

IV. DISCUSSION

Figure 5 reports on the state of the art in the field of MMIC and MIC frequency tripler conversion gain versus output frequency. It summarizes conversion gain achieved with the following technologies [5 to 9]: III-V FET and MESFET and BiCMOS (present SiGe tripler). It shows that, compared to GaAs technology, the BiCMOS SiGe one provides very interesting performance in term of conversion gain. Better results may be obtained only either with an hybrid solution [6] or with the penalty a higher power consumption [9].

We also have to outline that the optimum input power of our circuit is compatible with the output power delivered by a standard VCO designed using the same BiCMOS technology (P_{OUT}=0dBm, $L(f_M)$=-87 dBc/Hz for an offset frequency of 100 kHz) [10]. Moreover, the compatibility of this technology with a CMOS process will further allow to implement a "on chip" millimeter wave synthesizer having a very high frequency resolution.

Therefore phase noise investigations have been completed in order to address the capabilities of such a circuit to generate high spectral purity signals in the millimeter wave range. A predicted additive phase noise in the range of –143 dBc/Hz at an offset frequency of 100 kHz, is a very promising performance (thanks to the outstanding 1/f noise properties of SiGe HBT's) and demonstrates that this kind of circuit could fit the requirements for low phase noise signal generation in the millimeter wave range.

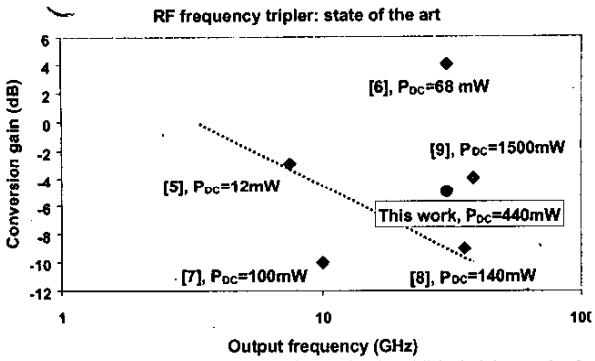

Fig. 5: Conversion gain vs. frequency for previously published triplers made of III-V transistors (hybrid or MMIC) compared to our work (SiGe MMIC)

V. VCO DESIGN

In order to get ready for the future monolithic assembly of an X band VCO with the frequency tripler, we have developed the 10 GHz VCO shown in figure 6.

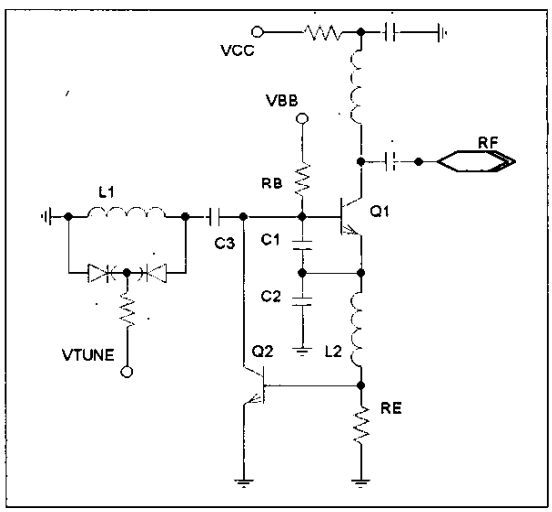

Fig. 6: Circuit's topology of VCO circuit.

This circuit uses a noise degeneration device [10, 11] in order to reduce the phase noise. Transistor Q_2 and resistors R_B, R_E perform this function by reducing the low frequency noise voltage at the base-emitter junction of Q_1. The Colpitts circuit is realized with transistor Q_1, capacitors C_1, C_2 and C_3, inductor L_1 and varactors. Inductor L_2 is used to cancel

the noise degeneration at high frequency in order to get rid of frequency stability problems. Theoretical studies and measurements, that have been performed on similar VCO circuit, have already been reported [10]: chip size is 830x960 μm^2, supply voltage and total power consumption of this circuit are respectively equal to 5 Volts and 460 mW. Figure 7 shows the measured VCO's output signal frequency versus tuning voltage. The circuit exhibits a maximum frequency tuning range of about 800 MHz and a maximum tuning sensitivity of 120 MHz/V for a tuning voltage range under 3 Volts.

Figure 8 reports the measured output power and phase noise (at a frequency offset of 100 kHz) versus tuning voltage. It shows that phase noise ranges between -74 and -87 dBc/Hz and that output power ranges from -4 to -8 dBm.

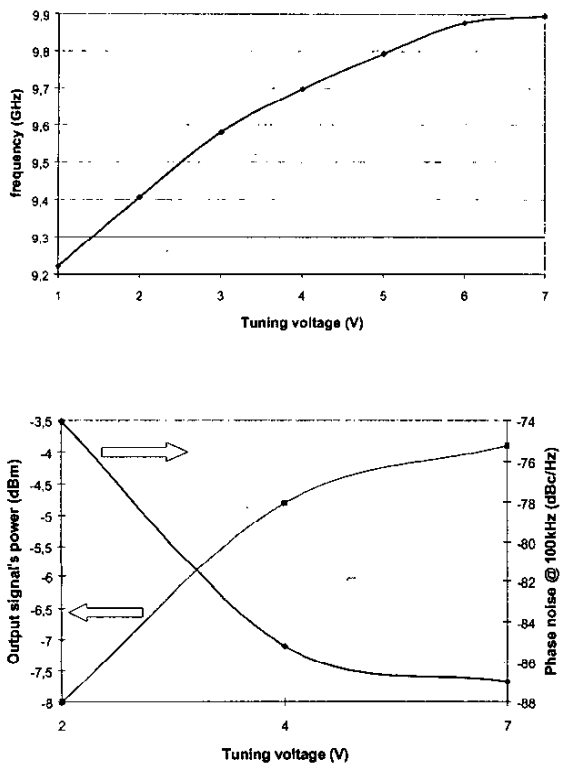

Fig. 8: Measured VCO output power (left) and phase noise (@ 100kHz offset from 10GHz carrier) measured vs. tuning voltage.

V CONCLUSION

A SiGe BiCMOS 30 GHz frequency tripler was successfully designed, fabricated and tested for future implementation in a millimeter wave synthesizer. It uses a low complexity 0.35 µm BiCMOS SiGe technology initially aimed at L and S-band applications. It nevertheless achieves attractive performance (thanks to a differential arrangement) such as a -5 dB conversion gain and a 7 dBc harmonics rejection for a power consumption of 440 mW at a voltage supply of 7 volts. Moreover an additive phase noise in the range of –140 dBc/Hz at an offset of 100 kHz from carrier is anticipated. The size of the circuit is about 0.4 mm^2 if microwave probe pads are not considered.

Furthermore an X-band VCO circuit, able to drive the tripler, was also designed, fabricated and measured. The chip size is similar to the previous one. Its total power consumption is 460mW for a 5 Volts supply voltage. Its output power is about – 5 dBm and its measured maximum frequency tuning range is 800 MHz (0 to 7V tuning volatage). It achieves a minimum -87 dBc/Hz phase noise, at a frequency offset of 100 kHz.

These results are encouraging for the future development of a low phase noise 30 GHz source. So, the VCO and tripler integration on a single chip is near completion. Furthermore, a new balanced version of these circuits is under design at this time, in order to improve conversion gain and, above all, harmonics rejection.

This paper finally demonstrates that a low complexity 0.35µm BiCMOS SiGe technology has also capabilities for advanced integrated circuit design in the millimeter wave range.

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